

IN THE CLAIMS:

CLAIMS

Please cancel claims 3, 21, 36.

Please amend the claims as follows:

A3 Sub 1
1. (Once Amended) An interface to transfer data directly between a first hub and a second hub within a computer system, comprising:
3 a data signal path to transmit data in packets via split transactions; and
4 a set of command signals, wherein said interface provides a point-to-point
5 connection between said first hub and said second hub, exclusive of an external
6 bus connected directly to the interface.

1 3. (Cancelled)

A3 Sub 2
19. (Once Amended) An interface to transfer data directly between a first hub and a second hub within a computer system, comprising:
3 a first means for transmitting data between said first hub and said second hub in
4 packets via split transactions; and
5 a second means for transmitting command signals, wherein said interface
6 provides a point-to-point connection between said first hub and said second hub,
7 exclusive of an external bus connected directly to the interface.

1 21. (Cancelled)

A3 Sub 3
1 35. (Once Amended) An interface to transfer data between a first hub and a second hub
2 within a computer system, comprising:
3 a set of data signals and a pair of source synchronous strobe signals, said data
4 signals transmit data in packets via split transactions, said packets including a request

5 <packet and completion packet, said request packet including a transaction descriptor;

6 and

7 a set of command signals including unidirectional arbitration signal and a

8 common clock signal, wherein said interface provides a point-to-point connection

9 between said first hub and said second hub, exclusive of an external bus connected

10 directly to the point-to-point connection.

1 36. (Canceled)

1 37. ~~An interface to transfer data between a memory controller hub and an input/output~~

2 (I/O) hub of a chipset within a computer system, comprising:

3 a bi-directional data signal path and a pair of source synchronous strobe signals,

4 said data signal path transmits data in packets via split transactions, said packets

5 including a request packet and completion packet, said request packet including a

6 transaction descriptor ; and

7 a set of command signals including unidirectional arbitration signal, a bi-

8 directional stop signal, a system reset signal, a common clock signal, and a voltage

9 reference signal.